AD1847 SoundPort Codec - DSP Interface Training

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AD18xx Training Goals

- Understand Basic Sigma-Delta Converter Technology Concepts
- To gain knowledge of our AD18xx product portfolio in order to provide front level of support for AD18xx requests
- Understand the DSP assembly driver source code for our more popular codecs
- Become aware of available AD18xx support documentation and drivers that will make your job much easier in supporting customers

Section 2

Overview of AD18xx Technology, Specifications and Applications

What is a Codec Anyway??

- A DSP only processes digital signals. These digital signals are derived from generated from “real-world” analog signals. A DSP typically processes input from and ADC and sends the output data to a DAC. This ADC/DAC process combo is the DSP’s interface to the “real world”.
- **CODEC** is short for COder/DECoder, which is another way of saying ADC/DAC. Thus, a CODEC is an ADC/DAC integrated on a single chip. But what makes codecs superior from regular converters is that they are programmable. A DSP has the ability to program various codec parameters for a particular application such as changing the sampling rate, the volume of the input signal, and selecting the source/destination for where the data will be collected/returned. The programming of a codec is done via it’s internal (indirect) registers.

What does it consist of ??

- In the early days of digital audio, the cost and size of system hardware needed to implement high-fidelity audio was not practical. A typical digital audio system separate A/D and D/A converters, oscillators, amplifiers, digital filter chips, and a DSP. These components added up to a larger, relatively expensive system.

- Thus, an AD184x CODEC was designed to incorporate on chip:
  - 16-bit ADC,
  - 16-bit DAC,
  - on-chip antialiasing and anti-imaging filters (hardcoded DSP functions),
  - programmable gain amplifiers on multiple channels of input and output, as well as,
  - programmable sampling rates.

AD18XX Audio Codecs

ADI's Audio Codecs Were Designed to Service the Data Conversion Needs of 3 Key Markets:

Consumer Audio
Professional Audio
Computer Audio

The AD1847 was originally designed for use on Compaq Computer sound cards. What ADI did not forsee is that many of the codecs such as the AD1847 that were designed to target the computer audio market were being designed into DSP audio applications, or even for embedded control system applications.

Key Specifications and Selling Features of Audio Converters:

Specification	**Selling Features**
Signal-to-Noise Ratio	Oversampling Rate
Total Harmonic Distortion	Modulator Design
Passband Ripple	Digital Filter Design
Stopband Attenuation	Performance
	Sound Quality

Important AD18xx Data Sheet Specifications

- **Analog Input** - Full Scale Input Voltage, Input Impedance and Input Capacitance
- **Analog Output** - Full Scale Output Voltage, Output Impedance, Output Capacitance, Current Drive
- **Gain** and **Attenuation** parameters (dB ranges)
- **Digital Decimation and Interpolation Filters** - passband, stopband, passband ripple, group delay...
- **ADCs and DACs** - Resolution 16 bits, signal-to-noise ratio (SNR), total harmonic distortion (THD), crosstalk, offset error, gain error...
- **Power Supply** - Analog and Digital Supply voltages and currents, powerdown, power supply rejection

AD18xx Data Sheet Definitions

- **Sigma-Delta Technology**: These types of ADCs and DACs provide very high resolution by oversampling and modulation (feedback integration). It utilizes low-performange analog circuitry by shifting the burden to the digital CMOS circuitry. This method has become an attractive choice for moderate-cost dedicated audio applications.
- **Dynamic Specifications**: These refer to the AC performance specifications. Included are S/N ratio, THD, passband ripple, stopband attenuation.

More AD18xx Definitions

- **Signal-to-noise Ratio (S/N):** This is the ratio of the input signal S to the background noise N in a system. For an ideal A/D converter with a sine wave input, the SNR related to the resolution n is

  SNR(RMS) = 6.02n + 1.76 dB

- **Total Harmonic Distortion + Noise (THD+N):** The ratio of the root-mean-square value of a full-scale fundamental input signal to the rms sum of all other spectral components in the passband, expressed in decibles (dB) and percentage.
- **Quantization Error:** All ADCs will have at least a minimum error as a result of the discrete or finite specs that represent the analog input, and this error is directly proportional to the resolution.

  Quantization Error = +/- .5 LSB

- **(Spurious Free) Dynamic Range:** This is the ratio of the full-scale input or output signal to the (highest harmonic) or spurious input/output noise component amplitude. Essentially, this is an indication of how far it is possible to go below the full-scale input signal without hitting noise or distortion. This is usually measured from 0 to 20 kHz and is expressed in decibels (dB). Dynamic range is measured with a -60 dB input signal and is calculated as follows:

  Dynamic Range = (S/[THD+N]) + 60 dB

  Note: Spurious harmonics are below the noise with a -60 dB input, so the noise level establishes the dynamic range. This is the recommendation of AES and EIAJ.

- **Total Harmonic Distortion:** A very important specification in audio systems, the THD is defined to be the RMS (root-mean-square) ratio of the sum of all spectral components (harmonic distortion amplitudes) to the original full-scale input amplitude. It is caused by the A/D converter nonlinearities.

- **Passive Support Components:** Codecs will end up depending on the passive components (resistors and capacitors) that surround them for accuracy and stability. The components should be chosen as recommended by the data sheet, or the codec perfomance can be severly affected.

- **Intermodulation Distortion (IMD)**: When two different-frequency signals are present, there will be an interaction caused by the A/D nonlinearity that generates additional frequency components. These additional frequencies will consist of the sum and difference between the original input frequencies and their harmonics.

- **Gain Error**: This is also the *full-scale error*, and it refers to the difference beween the input that produces a full-scale code and the ideal voltage, expressed in least significant bits. This is also expresses as a percentage of the actual output to the expected output.

- **Offset Error (zero error):** Midpoint between converter shresholds to the ideal response in LSBs.

- **Group Delay:** Intuitively, the time interval required for an input pulse to appear at the converter's output, expressed in seconds (s). More precisely, the derivative of radian phase with respect to radian frequency at a given frequency.

- **Group Delay Variation:** The difference in group delays at different input frequencies. Specified as the difference between the largest and the smallest group delays in the passband, expressed in microseconds (us).

- **Crosstalk (EIAJ method):** Ratio of response on one channel with a zero input to a full-scale 1KHz sine-wave input on the other channel, expressed in dB.
- **Gain Drift:** Change in response to a near full-scale input with a change in temperature, expressed as parts-per-million (ppm) per degree Celcius.
- **Interchannel Gain Mismatch:** With identical near full-scale inputs, the ratio of outputs of the two stereo channels, expressed in decibels.
- **Interchannel Phase Deviation:** Difference in output sampling times between stereo channels, expressed as a phase difference in degrees between 1 kHz inputs.
- **Power Supply Rejection:** With zero input, signal present at the ouptut when a 300 mV p-p signal is applied to power supply pins, expressed in decibels of full scale.
- **Midscale Offset Error:** Output response to a midscale DC input, expressed in least significant bits (LSBs).

- **Passband:** The region of the frequency spectrun unaffected by the attenuation of the digital interpolation filter.
- **Passband Ripple:** The peak-to-peak variation in amplitude response from equal-amplitude input signal frequencies within the passband, expressed in decibles.
- **Stopband:** The region of the frequency spectrum attenuated by the digital interpolation filter to the degree specified by “stopband attenuation.”
- **Nyquist Frequency:** An implication of the sampling theorem, the “Nyquist Frequency” of a converter is that input frequency which is one-half the sampling frequency of the converter.
- **Bandwidth:** The full opwer bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is redyced by 3 dB for a full-scale input.
- **Transport Delay:** The time interval between when an impulse is applied to the converters input and when the output starts to be affected by this impulse, expressedin millisecons(ms). T. Del is indendent of frequency.

What is considered ‘High Fidelity’ Audio ??

- People often refer to ‘CD-quality’ meaning high dynamic range. Some comparisons:

Audio Application	**Typical Signal Quality**
AM Radio	48 dB
Analog Broadcast TV	60 dB
FM Radio	70 dB
Video Camcorder	75 dB
ADI SoundPort Codecs	80 dB
Digital Broadcast TV	85 dB
Mini-Disk Player	90 dB
CD Player	92 dB
Digital Audio Tape (DAT)	110 dB

Sigma Delta - What is It?

- **Sigma Delta Converter -** can be referred to as an oversampling converter. Sigma Delta Codecs sample the input signal at a much higher rate than the maximum input frequency. Usually the sampling rate is 64, 128, 256 or 512 times faster.

- A **Sigma Delta Converter** Quantizes an analog signal with a very low resolution (1 bit) and a very high sampling rate (> 2 MHz). With the use of oversampling techniques and digital filtering, the sampling rate is reduced (ex, 8 khz) and the resolution is increased (16 bits).

  Thus, a sigma-delta converter can be thought of as one which samples an analog signal at one rate producing digital data and resamplesthe digital data at another rate.

Sigma Delta Converter Functions

The Sigma Delta ADC operation consist of:

- oversampling
- noise-spectrum shaping (using a Sigma Delta Modulator)
- digital filtering
- decimation

Interpolation/Decimation Filters

- The main difference between Sigma Delta ADCs and DACs on the codecs and digital audio products lies in the rate of the output signal.
- In the ADC section, **decimation** is used to reduce the high-frequency low-resolution pulses to lower-frequency, higher-resolution words.
- Sigma Delta DACs, on the other hand, do the reverse. Here a process called **interpolation** is performed that samples the digital outputs at a high rate. Note that a low-resolution digital code is samples multiple times at a high rate. This effectively produces a high-resolution/frequency output that is easily low-pass filtered for an analog output.

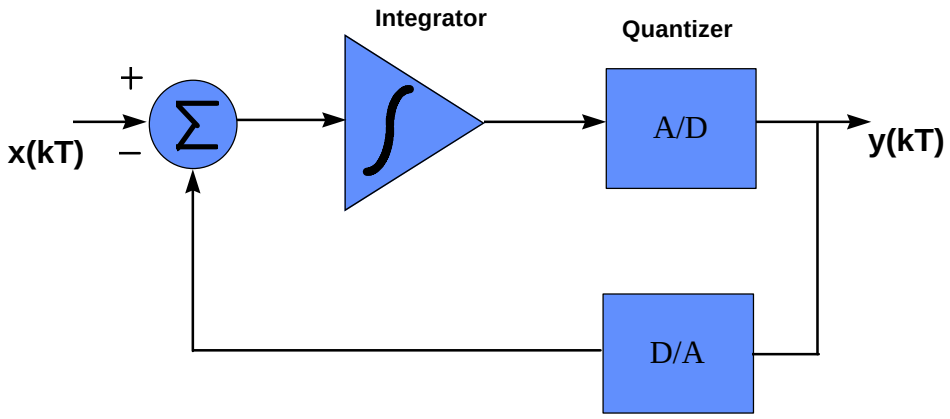
Sigma Delta - Decimation

- **Decimation** - The process of converting short words at high frequency to longer words at a slower rate. With the input signal oversampled at a very high rate, reducing the final output code frequency will make the computations more manageable. This reduces the effective sampling rate at the ADC output
- **Decimation** greatly reduces the complexity and speed requirements of the mathematical operations. If the number of computations per sample is reduces, the processor MAC requirements will be relaxed, thus resulting in a lower-cost design and possible higher performace due to less internal noise from high-frequency digital switching.
- Decimation is often done simultaneous with the filtering.

Interpolation

- The Sigma-Delta method is used also in codecs to create a high-performace DAC by applying a technique referred to as **interpolation**. This basically increases the output frequency of a low-resolution analog output.
- Done in conjunction with post-filtering. The net effect significantly improves the resolution and makes the DAC output easier to filter.

First Order S/D Modulator Block Diagram



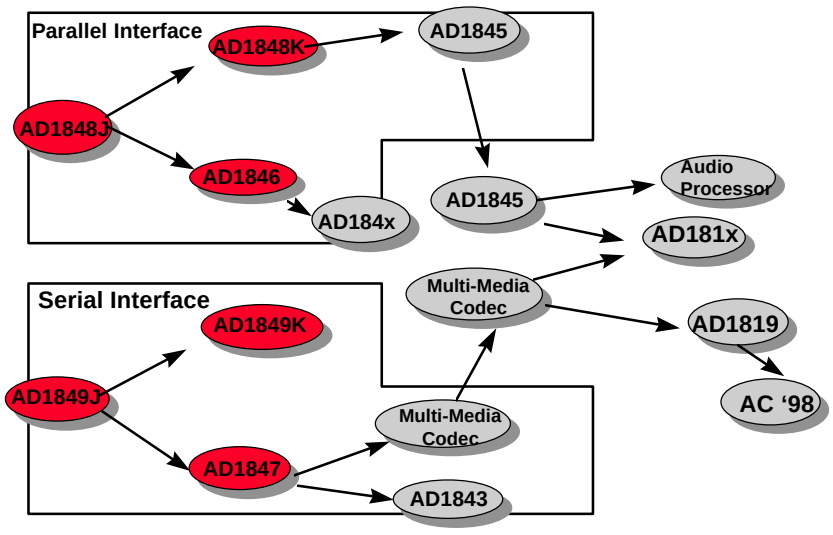
Modulator Consists of:

- an integrator
- a quantizer (comparator for 1 bit)
- feedback loop with D/A (switch for 1 bit). Since the conversion is performed with a 1 bit of quantization, there is a considerable amount of quantization error. The erroneous output is converted back to an analog signal with the D/A and fed back to the summing node where it is subtracted from the input signal to get quantization error value.

Section 2

AD1847 SoundPort Codec

AD184x Codec Roadmap



AD18XX Audio Codecs

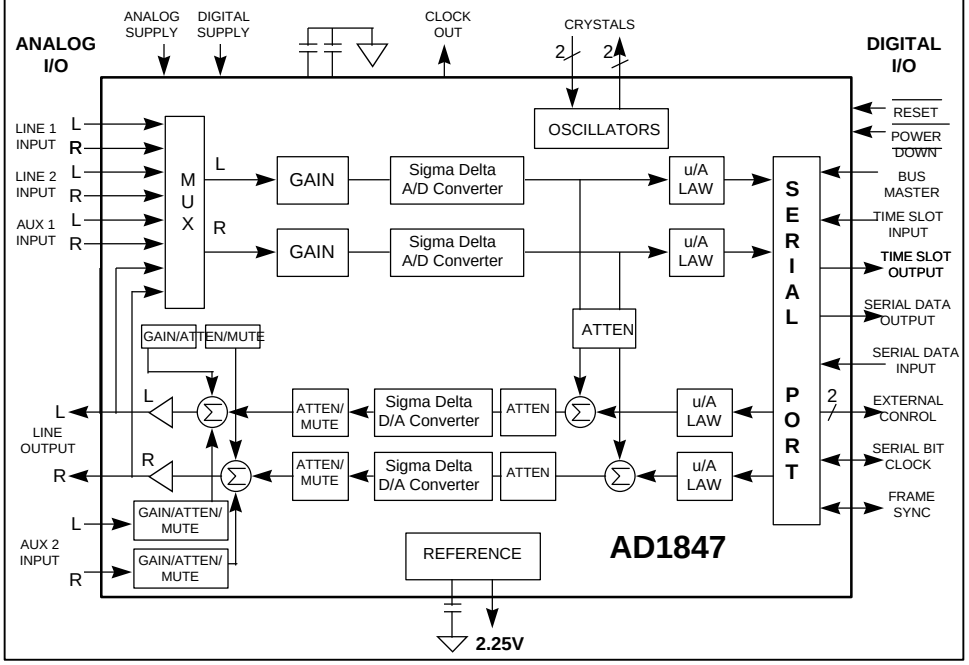
Example Applications

- Personal Computer Motherboards
- Add-in Sound Cards for Computer Audio
- Voice Annotation
- Speech synthesis
- Voice/Speech Recognition
- Digital Audio Amplifiers, Embedded Audio Systems
- High-Performace Compact Disc Players
- Musical Instruments, Audio Effects Processors
- Digital Mixing Consoles
- Used with ADSP-21XX Family DSPs Can Provide Advanced Audio Capabilities such as: Compression, 2-speaker 3D Effects, Audio Equalization, Reverb...

AD1847 Feature Summary

- Serial Port Sound Port 16-bit Stereo Codec
- Enables Industry Standard DSP Multimedia Architectures
- 70 dB Dynamic Range, -72 dB THD+N
- 44-Lead PLCC and TQFP Package Options
- Developed with Compaq Computer Corporation
- Multiple Channels of Stereo Input and Output
- Analog and Digital Signal Mixing
- On-Chip Signal Filters: Digital Interpolation; Analog Output Low-Pass
- Sample Rates from 5.5 to 48 kHz
- Serial Digital Interface Compatible with ADSP-21XX/21XXX Family DSP

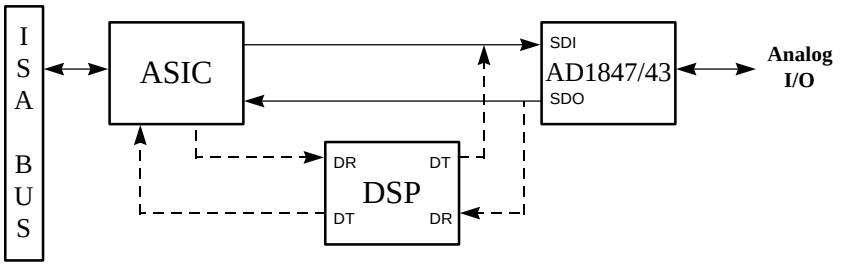
AD1847 Block Diagram



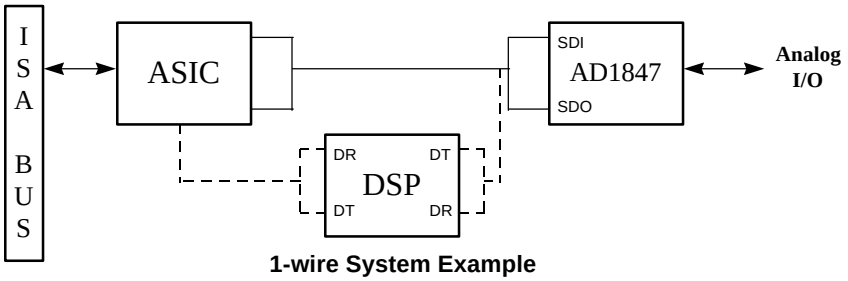
AD1847 CODEC Interface

- Stereo analog I/O through AD1847 CODEC
- AD1847 is a programmable device
  - Sampling rates: 5.5kHz - 48kHz
  - Input selection
  - Input/Output Gain/Attenuation
  - Mixing
- DSP Serial Interface Recommendation
  - Multichannel mode data stream
  - Uses Autobuffering

Example PC System Architecures

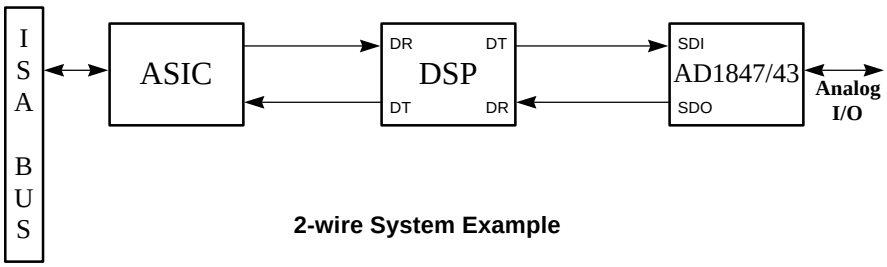


2-wire System Example

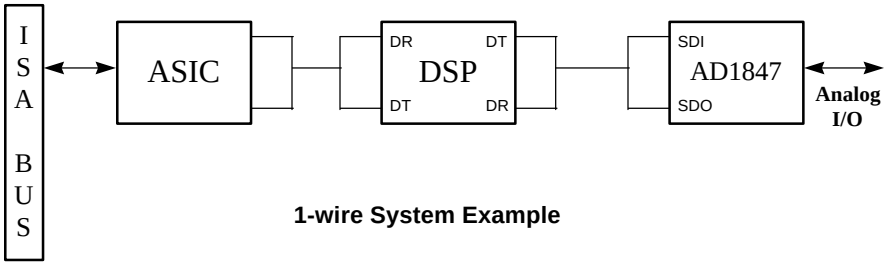


1-wire System Example

Example PC System Architectures



2-wire System Example



1-wire System Example

Introduction to the AD1847 Digital Serial Interfaces

Interfacing to the AD1847 and AD1843 Serial Ports

- AD1847AD1843 serial port is very different from the serial port on the AD1849
  - AD1849 is based on the Concentrated Highway Interface (CHI)
  - AD1847/AD1832 is based on DSP synchronous serial ports (SPORTs)

- AD1847 and AD1843 serial ports implement a **Time Division Multiplexed** (TDM) serial bus
  - Supports either 32 (FRS bit = LO) or 16 (FRS bit=HI) 16-bit time slots
    - ADSP-21xx SPORT0 can be programmed for either 24 or 32 16-bit timeslots - so use FRS=LO (cannot use the ADSP-2105, no SPORT0)
    - ADSP-2106x SPORTs can be programmed for 3 to 32 timeslots - so FRS can be either LO or HI
    - Motorola 5600x Port C configured as the Synchronous Serial Interface (SSI) operating in netwrok mode can be programmed to use 2 to 32 timslots
    - An AD1847 is a TDM bus slave (accepts external SCLK and FS) only in daisy-chained multiple codec systems

Interfacing to the AD1847 and AD1843 Serial Ports

- AD1847 systems can be implemented as either **1-wire**(simplex, bidirectional) [TSSEL=LO] or **2-wire** (duplex, unidirectional) [TSSEL=HI]
- Easiest interface design uses indirect register bit states assigned by default after reset: FRS = LO (32 time slots) and TSSEL=LO (1-wire)
- AD1843 systems can only be implemented in 2-wire mode. Indirect register states assigm FRS=LO (32 time slots) after reset. Since there are more timeslots that are active in any given frame vs. the AD1847, 1-wire mode is not a practical solution, especially for multiple codec systems.
- Notice that the AD1847 and AD1843 serial port functionality is identical in operation. Thus, the DSP serial port's memory mapped registers are set up exactly the same with exception to multichannel timeslot enables.

AD1847 Data Stream & DSP Relationship

- AD1847 Generates SCLK and Frame Synch signals
- For stereo operation, three words/sample are needed
  - Control / Status [DM(tx_buf), DM(rx_buf)]
  - Left channel data [DM(tx_buf + 1), DM(rx_buf +1)]
  - Right channel data [DM(tx_buf +2), DM(rx_buf+2)]
- DSP gets/puts information and data ideally from a buffer that is assigned to the SPORT0's transmit and receive autobuffers. Autobuffering in multichannel mode is the easiest way to send/recieve data since it reduces interrupt overhead, and the user need not worry what current timeslot the data is assigned to . An interrupt will occur when all 3 words are transmitted/recieved in the current frame (i.e., circular buffer points to the top of the buffer.

AD1847 Control Register Mapping With TSSEL = 0

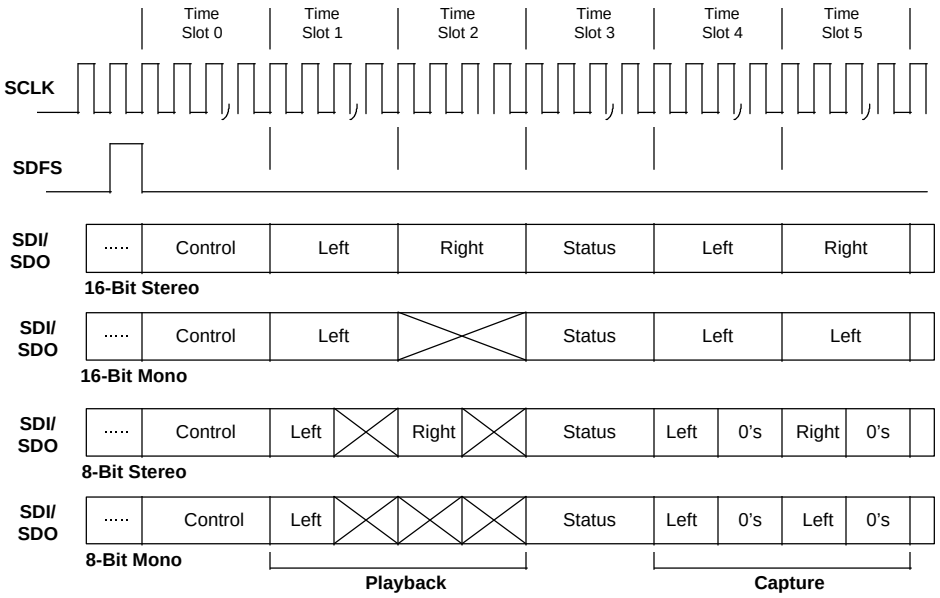
Slot	Direct (Control) Register Name
0	Control Word Input
1	Left Playback Data Input
2	Right Playback Data Input
3	Status Word/Index Readback Output
4	Left Capture Data Output
5	Right Capture Data Output

AD1847 Control Register Mapping With TSSEL = 1

Slot	Direct (Control) Register Name
0	Control Word Input
1	Left Playback Data Input
2	Right Playback Data Input
0	Status Word/Index Readback Output
1	Left Capture Data Output
2	Right Capture Data Output

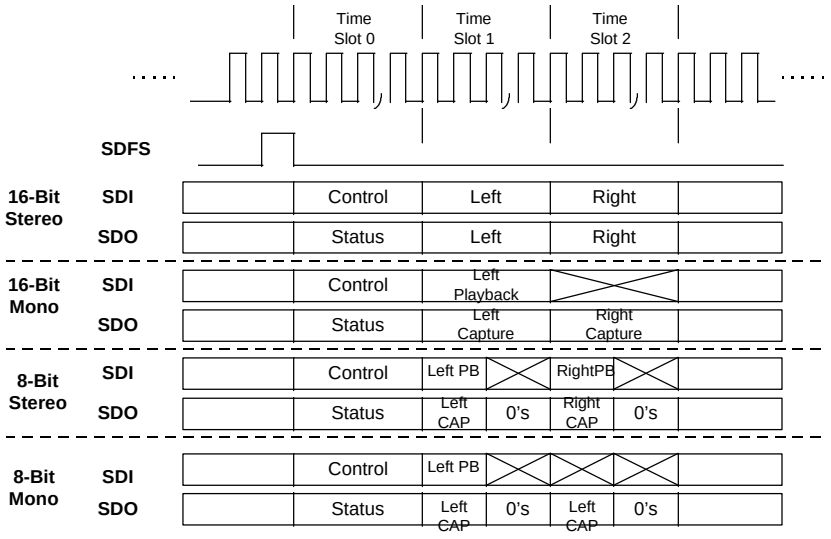
AD1847 Serial Data Format

1-wire System (TSSEL=0)



AD1847 Serial Data Format

2-wire System (TSSEL=0)



AD1847 Serial Port Signals

- **Serial Clock - SCLK**
  - Bidirectional: output when AD1847 is serial bus master, input when slave
  - Fixed at 12.288 MHz when XTAL1 selected, fixed at 11.2896 MHz when XTAL2 selected
- **Serial Data Input - SDI**
  - Input that received 16-bit, MSB-first Control Word and Playback Data
- **Serial Data Output - SDO**
  - Output that transmits 16-bit, MSB-first Status Word or Index Readback and Capture Data
- **Serial DataFrame Synch - SDFS**
  - Bidirectional: output when AD1847 is serial bus master, input when slave
  - If FRS=0(reset default), frame sync frequency is one half the selected sample frequency with two sample per frame
  - If FRS=1, frame sync frequency matches the selected sample frequency with one sample per frame
- **Time Slot Input - TSI**
  - Indicates to the AD1847 that it should use the next three (TSSEL=1) or the next six (TSSEL = 0) time slots, then assert TSO to activate the next codec down the daisy-chain
  - TSI must be grounded in single codec systems or on the master codec in daisy-chained multiple codec systems
- **Time Slot Output - TSO**
  - Asserted HI coincidentally with the LSB of the last time slot used by the AD1847

AD1847 Serial Port Notes

- The serial clock (SCLK) runs continously
- The frequency of SCLK is fixed (either 12.288 MHz or 11.2896 MHz), but the FSYNC frequency is a function of the programmed sample rate, so the numver or SCLK periods per frame is also a functin of the programmed sample rate.
- With FRS=0 (32 slots per frame), slots are paired (0 with 16, 1 with 17, 2 with 18, etc.)
  - Assuming 1-wire system, slots 0 and 16 are Control Words for consecutive samples to same codec; slots 1 and 17 are Left Playback Data for consecutive samples to same codec; etc.
- Time slot allocation in daisy-chained multiple codec systems is determined by physical location (i.e., the connections between the Time Slot Out [TS0] and the Time Slot In [TSI] signals).
- Due to the efficiency of slot utilization, 2-wire systems (TSSEL=1) is a better choice for systems which include a DSP chip on the TDM bus.
- The Serial Data Output (SDO) pin output is normally three-stated except during output slots, during which time it is enabled.

AD1847 Control Register Mapping

- The AD1847 has **six 16-bit direct registers** and **thirteen 8-bit indirect Index registers** accessible to the user from the serial port
- The Index registers are **accessed with indirect addressing** through the Control Word
- **RREQ** bit in the Control Word requests either Status Word transmitted (RREQ = 0) ir Index Readback transmitted (RREQ=1) from the AD1847
- **Index Readback uses Control Word format** (CLOR, MCE RREQ and IA3:IA0 are echoed from previous Control WOrd, and DATA7:DATA0 contains Index register data

AD1847 Index Register Bit Table

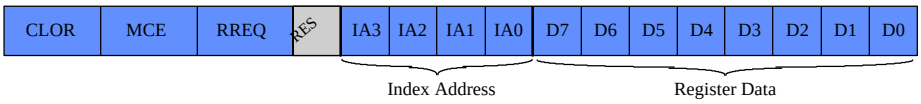
reset	7		5	4		2	1		prgm
00		LSS0	res		LIG3	LIG2		LIG0	
00		RSS0	res		RIG3	RIG2		RIG0	
80		res	res		LX1G3	LX1G2		LX1G0	
80		res	res		RX1G3	RX1G2		RX1G0	
80		res	res		LX2G3	LX2G2		LX2G0	
80		res	res		RX2G3	RX2G2		RX2G0	
80		res	LDA5		LDA3	LDA2		LDA0	
80		res	RDA5		RDA3	RDA2		RDA0	
00		FMT	C/L		CFS2	CFS1		CSL	
08		res	res		ACAL*	res		PEN	
00		XCTL0	CLKTS		res	res		res	
--		inval	inval		inval	inval		inval	
00		TSSEL	res		res	res		res	
00		DMA4	DMA3		DMA1	DMA0		DME	
--		inval	inval		inval	inval		inval	
--		inval	inval		inval	inval		inval	

*** - the Mode Change Enable bit of the Control Word**

AD1847 Index Register Table

Reg	Data Sheet Description		Addr
0	Left Input Control		
1	Right Input Control		
2	Left Auxiliary #1 Input Control		
3	Right Auxiliary #1 Input Control		
4	Left Auxiliary #2 Input Control		
5	Right Auxiliary #2 Input Control		
6	Left DAC Control		
7	Right DAC Control		
8	Data Format		
9	Interface Confiruration		
10	Pin Control		
11	reserved		
	Miscellanious Information		0x0C00
	Digital Mix Control		0x0D00
	reserved		
15			

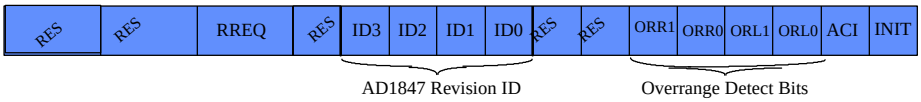
AD1847 Control Word



- **CLOR** - Clear Overrange: Used to clear overrange bits in status word
- **MCE** - Mode Change Enable: When set, allows access to protected registers for modification of sample rate, data format, and multichannel configuration
- **RREQ** - Read Request: Used to signify that the contents of a data register should be sent rather than the next status word
- **Index Address** - Address of the data register whose contents are to be modified (or read, if RREQ is valid)
- **Register Data** - 8 bit value used to program the specified register

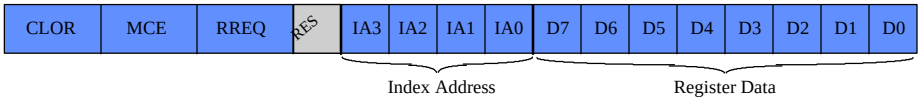
- Complete register specifications can be found in the AD1847 Data Sheet

AD1847 Status Word



- **RREQ** bit in the Control Word requests Status Word to be transmitted (RREQ = 0). This bit is reset LO for the status Word, echoing the RREQ=0 state written by the host in the previous control word
- **ACI** - Autocalibrate In-progress -- This bit indicates that an autocalibration is in progress or the Mode Chagne ENable state (MCE) state has been recently exited
- **INIT** - Initialization. This bit is an indication to the host that frame syncs will stop and the serial bus will be shut down.

AD1847 Index Readback Word



- Index Readback uses Control Word format (CLOR, MCE RREQ and IA3:IA0 are echoed from previous Control Word, and DATA7:DATA0 contains Index register data
- Indirectly addressed index register occurs in the following frame after a RREQ=1 occurs in the Control Word of the following frame

Miscellaneous Information Register (Index Address 12)

- Only be changed when AD1847 is in Mode Change Enable (MCE) state
- Changes updated at next SDFS boundary
- **TSSEL** - Transmit Slot Select - data bit #6
  - 0: Transmit on time slots 3,4,5. Used when SDI and SDO are tied together in 1-wire mode
  - 1: Transmit on slots 0,1,2. Used when SDI and SDO are independent inputs are tied
- **FRS** - Frame Size - data bit #7. This bit selects the number of time slots per frame

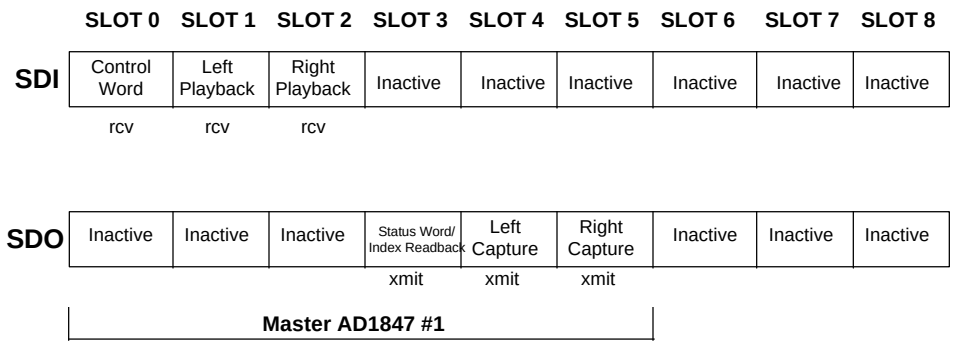
  0 - Selects 32 slots per frame (two samples per frame sync at half the sample rate

  1 - Selects 16 slots per frame (one sample per frame sync at the sample rate

AD1847 Control Register Defaults

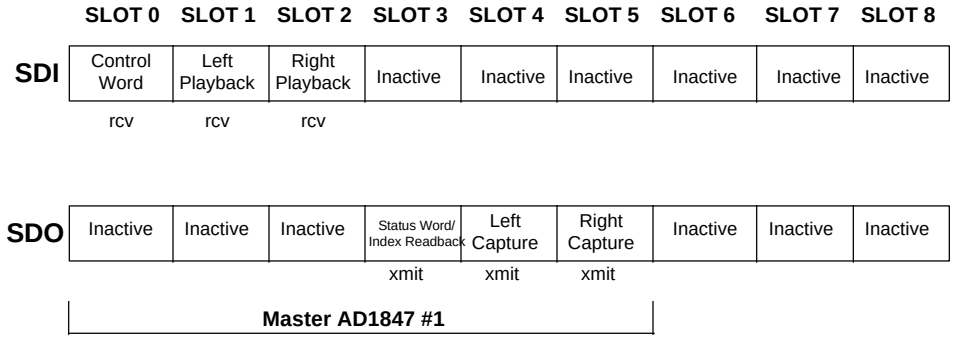
- Register Reset defaults include TSSEL = 0 and FRS = 0 in the Miscellaneous Information Register
  - **TSSEL = 0** means that the AD1847 will transmit status/index readback and capture data on slots 3,4 and 5, and is used when SDI and SDO are tied together in a 1-wire system
  - **FRS = 0** means that the AD1847 will operate with 32 slots per frame, i.e., two sample per frame sync.
- What if system design requires 2-wire support, or requires 16 slots per frame?
  - To bootstrap into TSSEL = 1 (i.e., 2-wire system), ASIC or DSP must transmit to AD1847 in slot 0 a Control Word with the MCE bit set HI, IA3:0="1100" to address the Miscellaneous Information Control Register, and DATA7:0="X1000000" to set TSSEL bit HI.
  - To bootstrap into FRS=1 (i.e., 16 slots per frame), ASIC or DSP must transmit to AD1847 in slot 0 a Control Word with the MCE bit set HI, IA3:0 = "1100" to address the Miscellaneous Information Index Register, and DATA7:0 = "1X000000" t set the FRS bit HI.
  - The only other requirement is that the ASIC or DSP must maintain the MCE bit set HI in slot 16, which is the Control Word of the second sample of the frame, so that the AD1847 does not initiate autocalibration.
  - At the next frame sync, the AD1847 will be reconfigured
- Note that the MCE bit does not have to be reset LO in order for changes to be updated!

Serial TDM Bus and Timslots
Single Codec “1-Wire” System



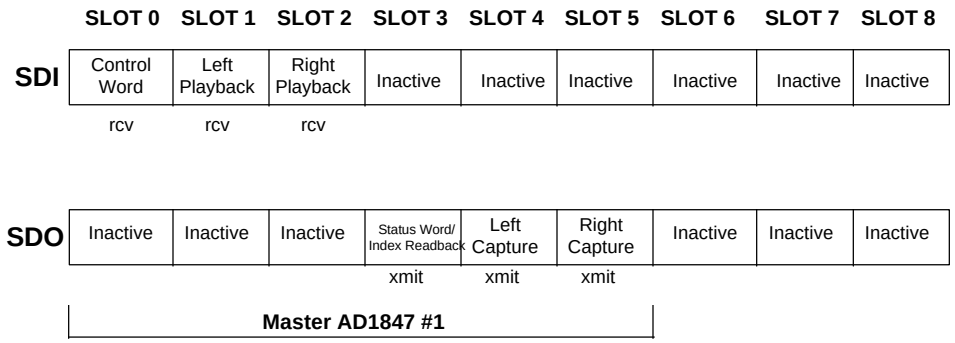
TSSEL = 0 “1-Wire” System

Serial TDM Bus and Timslots
Single Codec “1-Wire” System



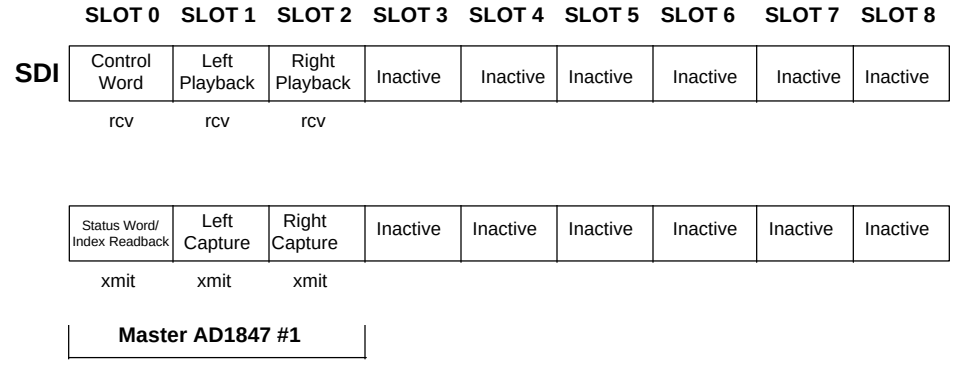
TSSEL = 0 “1-Wire” System

Serial TDM Bus and Timslots
Single Codec “1-Wire” System



TSSEL = 0 “1-Wire” System

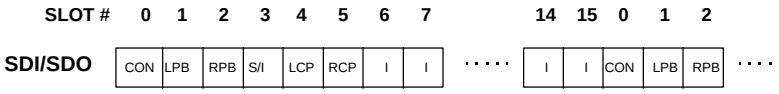
Serial TDM Bus and Timslots
Single Codec “2-Wire” System



TSSEL = 1 “2-Wire” System

Serial TDM Bus and Timeslots
4 Possible Configurations

Configuration # 1: 1-wire, 16 slots/frame, 1 sample/frame sync

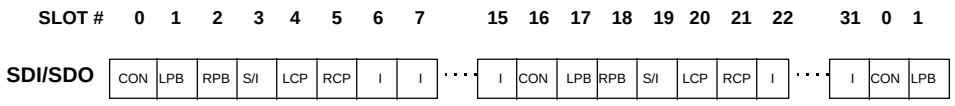


FRS = 1
TSSEL = 0
Single Codec System

CON = Control Word
LPB = Left Playback Data
RPB = Right Playback Data
S/I = Status Word/Index Readback
LCP = Left Capture Playback
RCP = Right Capture Data
I = Inactive

Serial TDM Bus and Timeslots
4 Possible Configurations

Configuration # 2: 1-wire, 32 slots/frame, 2 samples/frame sync

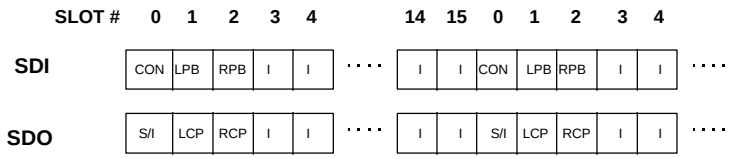


FRS = 0
TSSEL = 0
Single Codec System

CON = Control Word
LPB = Left Playback Data
RPB = Right Playback Data
S/I = Status Word/Index Readback
LCP = Left Capture Playback
RCP = Right Capture Data
I = Inactive

Serial TDM Bus and Timeslots
4 Possible Configurations

Configuration # 3: 2-wire, 16 slots/frame, 1 sample/frame sync

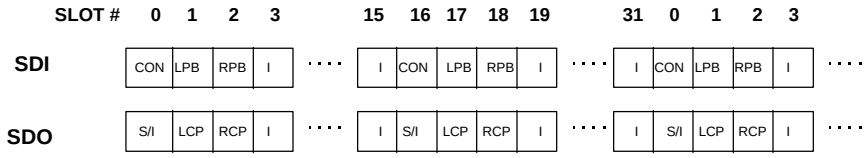


FRS = 1
TSSEL = 1
Single Codec System

CON = Control Word
LPB = Left Playback Data
RPB = Right Playback Data
S/I = Status Word/Index Readback
LCP = Left Capture Playback
RCP = Right Capture Data
I = Inactive

Serial TDM Bus and Timeslots
4 Possible Configurations

Configuration # 4: 2-wire, 32 slots/frame, 1 sample/frame sync



FRS = 1
TSSEL = 1
Single Codec System

CON = Control Word
LPB = Left Playback Data
RPB = Right Playback Data
S/I = Status Word/Index Readback
LCP = Left Capture Playback
RCP = Right Capture Data
I = Inactive

The AD1847 Frame Rate is **Not Directly Related** to the Sampling Rate at Which the Codec is Operating At !!!

Frames & Samples with respect to the Frame Sync

The AD1847 has a two-sample deep buffer to allow for slower sampling rates.

Since the AD1847's serial bit clock rate is fixed, the interval beween time slot 0 and time slot 16 is less that the sample period.

The pipelining is required to properly resolve the interface between the relatively fast fixed SCLK rate, and the relatively slow sample rates (and therefore frame sync rates) at which the AD1847 is capable of running. At low sample rates, two samples of data can be serviced in a fraction of a sample period.

Audio Frame/Frame Sync Relationship

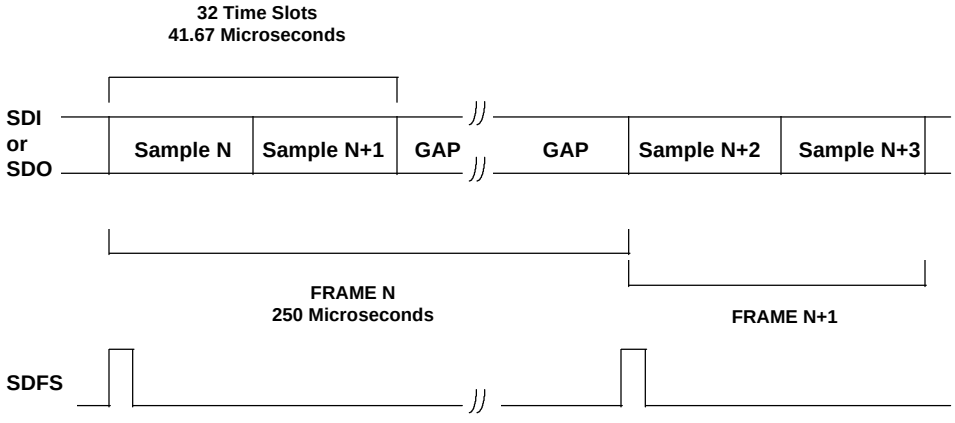
For example, at 8KHz sample rate, 32 time slots only take up 41.67 usec out of a 125 usec period.

(32 timeslots) x (16 bits per slot) x (1/12.288 MHz SCLK) = 41.67 usec

If the FRS bit is set to one, then the AD1847 sets up 16 time slots per frame (this bit can be set for other processors that support 16 TDM timeslots). For an 8kHz sampling rate, data is expected at 125 us. At that sampling rate, the serial bit clock produced by the AD1847 is 12.288 Mhz, yielding a time span between data samples of 20.83 us.

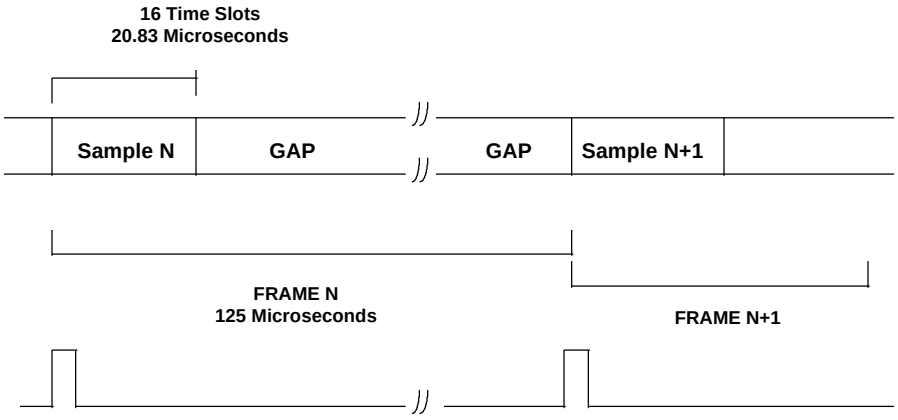
(16 words) x (16 bits/word) x (1/12.288 Mhz SCLK) = 20.83 usec.

Frames, Samples and Frame Syncs



FRS = 0 [32 Slots Per Frame, 2 Samples Per Frame Sync]
8 kHz Sample Rate Example

Frames, Samples and Frame Syncs

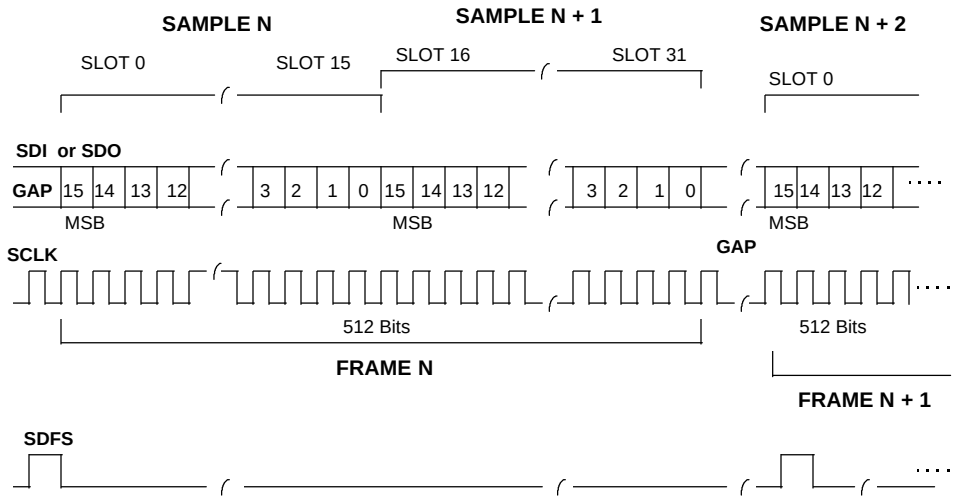


FRS = 1 [16 Slots Per Frame, 1 Samples Per Frame Sync]
8 kHz Sample Rate Example

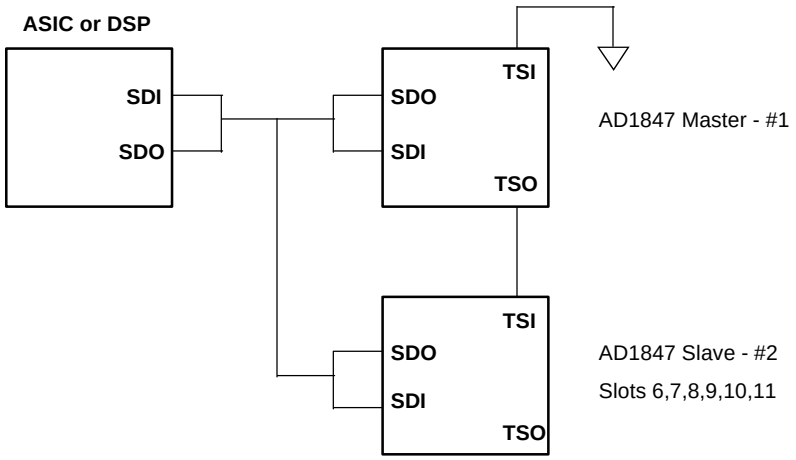
AD1847 Serial Port Timing Diagrams

Relationship between Audio Frames, Samples and Frame Syncs

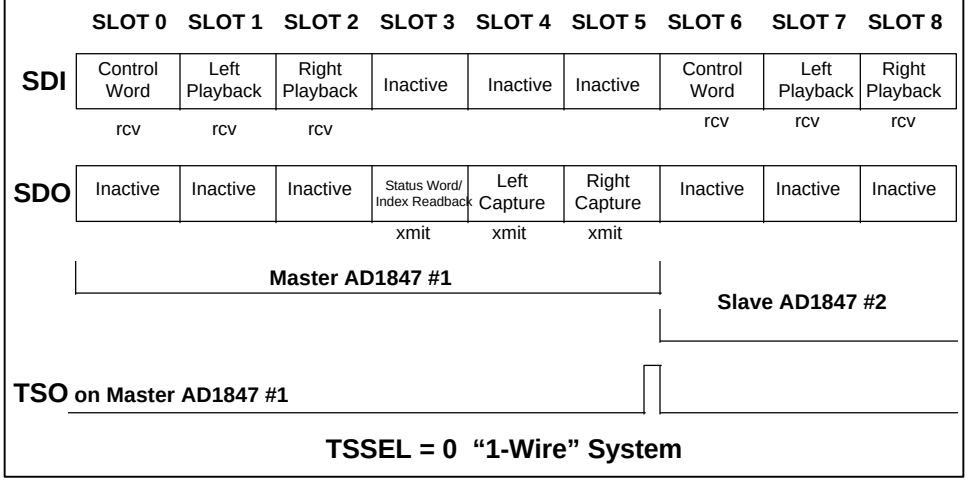
Low Sample Rate Example, FRS=0
[32 Slots per Frame, 2 Samples per Frame Sync]



Daisy-Chained Multiple Codec Systems
1-Wire Interface

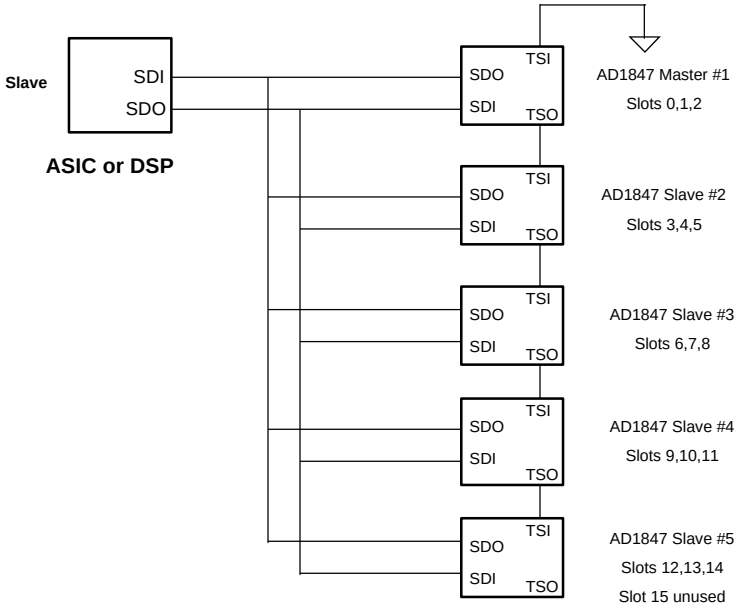


Daisy Chained Multiple Codec 1-Wire

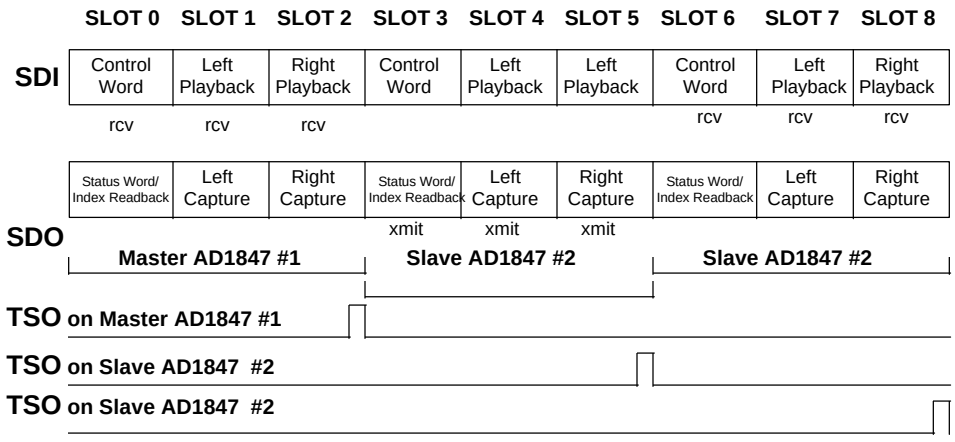


TSSEL = 0 "1-Wire" System

Daisy-Chained Multiple Codec Systems 2-Wire Interface

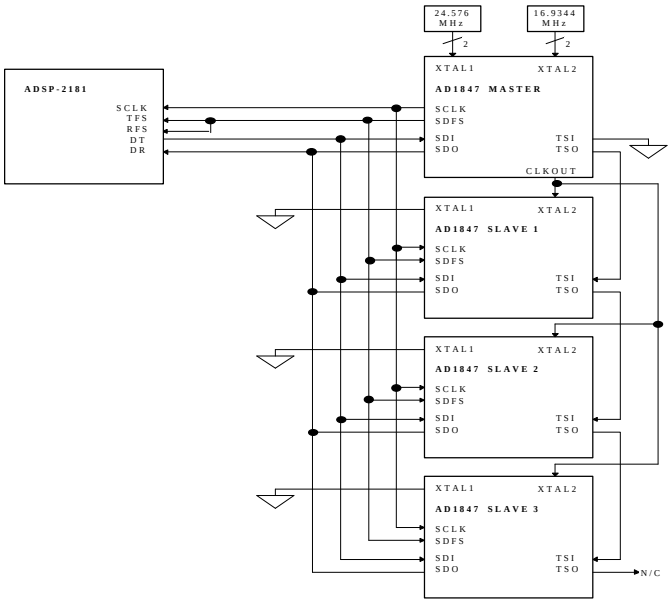


Daisy Chained Multiple Codec 1-Wire



TSSEL = 1 "2-Wire" System

Daisy Chaining Multiple AD1847s to the ADSP-2181

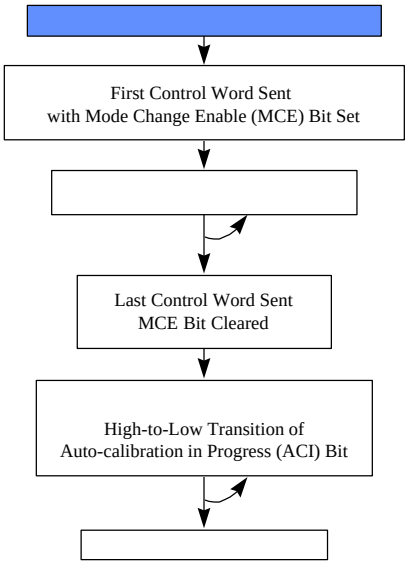


Programming the AD1847

What should the DSP Software Programmer do in order to

fully functional after a reset ??

AD1847 Initialization



AD1847 Autocalibration

The AD1847 has the ability to calibrate its ADCs and DACs for

measures the approximate input offset of the ADC at power up and stores the valuefor subtraction from the subsequent

- Mode Change Enable (MCE) state AND the ACAL bit in the Interface Configuration Register has been set.

The completion of the autocalibration sequence can be

the Status Word. This bit will be HI while the autocalibration is in prograss and LO once autocalibration has completed. The

AD1847 Start Up Sequence (Autocalibration Procedure)

- AD1847 must be reset after power-up! Tie RESET pin to system reset signal or to a DSP flag pin
- AD1847 will come out of reset with control registers containing defaults
- Bootstrap as necessary into TSSEL=1 or FRS=1 condition
- Maintain MCE=1 so that AD1847 does not initiate autocalibration, and use consecutive Control Words to establish desired control register setting (except for AUX1 and AUX2 mutes, which must be maintained HI, i.e., muted)
- Ensure that Autocalibrate Enable (ACAL) is HI (reset default)
- Send Control Word with MCE bit reset, causing the AD1847 to initiate autocalibration
- Poll Status Word for ACI LO, indicating that autocalibration is complete
- Unmute AUX1 and AUX2 inputs if desired
- AD1847 ready for normal operation

Example 21xx Family Code Fragment for AD1847 Initialization

```
ax0 = dm (i1, m1);              { start interrupt }
      tx0 = ax0;

check_init:
      ax0 = dm (stat_flag);     { wait for entire init }
      af = pass ax0;            { buffer to be sent to }
      if ne jump check_init;    { the codec          }

      ay0 = 2;
check_aci1:
      ax0 = dm (rx_buf);        { once initialized, wait for codec }
      ar = ax0 and ay0;         { to come out of autocalibration }
      if eq jump check_aci1;    { wait for bit set }

check_aci2:
      ax0 = dm (rx_buf);        { wait for bit clear }
      ar = ax0 and ay0;
      if ne jump check_aci2;
      idle;
```

```
ay0 = 0xbf3f;                   { unmute left DAC }
      ax0 = dm (init_cmds + 6);
      ar = ax0 AND ay0;
      dm (tx_buf) = ar;
      idle;

      ax0 = dm (init_cmds + 7);  { unmute right DAC }
      ar = ax0 AND ay0;
      dm (tx_buf) = ar;
      idle;
```

Programming the Index Registers via the SPORT0 Tx ISR

```
{-------------------------------------------------------------------------------
 -
 -  transmit interrupt used for Codec initialization
 -
 -------------------------------------------------------------------------------}
next_cmd:
      ena sec_reg;
      ax0 = dm (i3, m1);        { fetch next control word and }
      dm (tx_buf) = ax0;        { place in transmit slot 0    }
      ax0 = i3;
      ay0 = ^init_cmds;
      ar = ax0 - ay0;
      if gt rti;                { rti if more control words still waiting }
      ax0 = 0xaf00;             { else set done flag and }
      dm (tx_buf) = ax0;        { remove MCE if done initialization }
      ax0 = 0;
      dm (stat_flag) = ax0;     { reset status flag }
      rti;
```

Audio Loopback via SPORT0 Rx ISR (Passing Data from Rx to Tx)

```
{-----------------------------------------------------------------------------
 -
 -  receive interrupt used for loopback
 -
 -----------------------------------------------------------------------------}
input_samples:
       ena sec_reg;                    { use shadow register bank }
       mr0 = dm (rx_buf + 1);          { loopback inputs to outputs }
       mr1 = dm (rx_buf + 2);

       dm (tx_buf + 1) = mr0;
       dm (tx_buf + 2) = mr1;
      rti;
```

Section 5

AD18xx Applications Support Information

AD184x Documentation

Application Notes:

21xx Applications Manual, Vol 2 Ch 12 - Codec Interfaces:

ADSP-2105/AD1849 SoundPort Interface

ADSP-2111/AD1849 SoundPort Interface

ADSP-2101/AD1847 SoundPort Interface - Talkthru

EZ-KIT-LITE MIC2OUT.DSP -- ADSP-2181/AD1847 Talkthru Driver

BBS & FTP Site- AUX2OUT.DSP -- ADSP-2181/AD1843 Talkthru Driver

AN-387 AD1847 Serial-Port Interface Example for a Parallel Bus

AN-388 Using Sigma-Delta Converters - Part 1

AN-389 Using Sigma-Delta Converters - Part 2

AN-283 Sigma-Delta ADCs and DACs

AN-404 Considerations for Mixed Signal Circuit Board Design (How to Design a PCP Layout/Assembly Compatible with the AD1845 and CS4231 Codecs)

Application Notes (Preliminary Drafts)

AN-??? ADSP-2181 Serial Port Interface Example for the AD1816/AD1816A

AN-??? Interfacing the ADSP-2181 DSP to the AD1819 SoundPort Codec

AD184x Documentation

Engineer's Notes (Codec SoundBytes)

- Configuring the AD1847 as a Two-Wire Mode, 32-Slot System for ADI DSP Functionality
- ADSP-21xx Multichannel Slot Assignments for the AD1847
- Multiple Codec 2-Wire Mode Configuration
- AD1847/ADSP-2181 Daisy Chaining Tips & Tricks
- Daisy Chaining Multiple AD1847s to a DSP -Ground Plane Recommendations
- AD1847 Frame Sync and DSP Interrupts
- AD1847 Data Sheet Q & As
- Measuring the Dynamic Range and DAC Crosstalk of the AD1847
- AD1849K Jitter Requirements and Input Signal Coupling
- An AD1847/ADSP-2181 Loopback Example Using a Single Index Register
- AD1843/ADSP-2181 Autobuffering Timing Considerations
- AD1843 Programmer's Quick Reference
- AD1843/ADSP-2181 Loopback Example
- AD184x Sigma Delta Converters: How well do they work with DC inputs?

AD184x Documentation

White Papers

Integrating Serial Codecs into the PC

Interfacing to the AD1847 Serial Port

AD1847 Mafe Specification

Notes On DC Codec Operation

DSPatch Article: Sigma-Delta Conversion Technology